

Plug-in Gate-loop Compensators for Series-connected IGBT Drivers in a Solid-state Fault Current Limiter

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Abstract—A solid-state fault current limiter (SSFCL) is the key protective equipment in a direct current distribution network. In order to meet the high voltage requirements and reduce costs, implementing a SSFCL based on series-connected insulated gate bipolar transistors (IGBTs) is a promising approach. However, voltage unbalancing of IGBTs would be introduced if the gate-loops of the IGBTs are non-identical. In this paper, a plug-in gate-loop compensator with discrete gate voltage feedback and pulsewidth current compensation is proposed. The main merits are: 1) with the plug-in structure, the extra current sources only provide small power to fine-tune the gate-loop without affecting the functions provided by the commercial IGBT gate driver; 2) the gate-emitter voltages of IGBTs are compared with the preset thresholds to obtain control criterion, and the pulsewidths of the current sources are controlled for gate-loop compensation, thus both analog-digital and digital-analog converters are avoided; 3) the control law is easy to implement in FPGA, and is robust to voltage variation of power-loops. With the proposed compensator, the voltage unbalancing is alleviated immediately at the present switching cycle, and further eliminated cycle-by-cycle during the current limitation process. Experimental results verify the feasibility of the proposed compensator.

Index Terms—Current limitation, direct current distribution network, insulated gate bipolar transistors (IGBTs), voltage balancing.

I. INTRODUCTION

AS for the establishment of a power distribution network, using direct current (DC) has many advantages compared to that of alternating current (AC), such as less loss, larger capacity and so on [1]. However, the line current would be rising rapidly once a short-circuit fault occurs, which requires DC protective equipment to immediately limit the fault current. A solid-state fault current limiter (SSFCL), which can limit the fault current to a given level within a given period, is commonly adopted [2], [3]. For a medium or low voltage

DC distribution network, SSFCL based on series-connected insulated gate bipolar transistors (IGBTs) is a cost-efficient solution since the voltage rating of a single IGBT is limited. A typical application of SSFCLs is shown in Fig. 1. Several IGBTs are in series as a switch, and it is constantly on when the load or the lines in the downstream is under normal operation. Once the short-circuit in the load side occurs, the switch is operated under pulse-width modulation (PWM) to limit the fault current within a certain level. Such a fault current not only ensures the safety of the transmission lines, but also creates the operating conditions for the protective equipment (such as fuse or DC circuit breaker) near the load side.

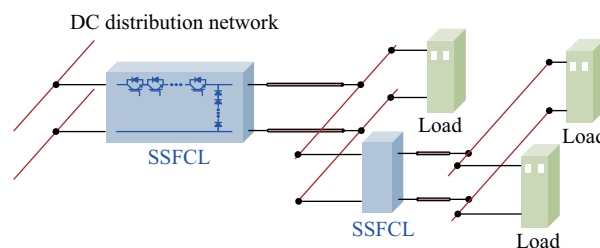


Fig. 1. Application example of the SSFCLs in a DC distribution network.

However, during the repetitive switching processes to limit the short current, voltage could be introduced in the series-connected IGBTs for two reasons: 1) the power-loops of the IGBTs are not identical and 2) the gate-loops of the IGBTs are not identical [4]. The former problem has been well documented, and can be solved by adding passive snubbers [5] or applying active gate driver technologies [6]–[23]. In order to reduce voltage unbalancing, some feedback from the power-loop should be acquired as control criterion in such active gate driver technologies. For example, references [6]–[11] fed back the clamp circuit current or the collector current, and [12]–[14] fed back the collector-emitter voltage for control; Reference [20] added an extra Miller capacitor and used its current to compensate the gate current. In addition to these analog methods, some digital methods were also proposed. In [21], the collector-emitter voltages of IGBTs were compared with some thresholds to generate discrete signals; in [22], [23], the voltages were sampled with analog-to-digital converters (ADCs); the latter problems, however, are generally solved by fine-tuning the gate-loop parameters to make the gate-

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emitter voltages as identical as possible. Such a trial-and-error method is burdensome when the amount of IGBTs is large, and is inconvenient and risky when the voltage level is high. Although the technologies in [22]–[24] were also able to control the gate-emitter voltages, they required analog-to-digital converters (ADCs) or digital-to-analog converters (DACs) as interfaces, which brought in extra circuit complexities; and they required a complete redesign of the gate drivers, losing many benefits of the mature commercial gate drivers.

To remain the benefits of a commercial IGBT gate driver and realize fast and robust gate-loop compensation, a FPGA-based, plug-in gate-loop compensator with discrete gate voltage feedback and pulse width current compensation is proposed in this paper. The gate-loop compensation is automatic without trial-and-error, and it is especially suitable for SSFCL applications:

1) The plug-in structure ensures that the commercial IGBT gate driver with main driving power and powerful protection is still available. Only extra current sources with small power are added to fine-tune the gate-emitter voltage.

2) The gate-emitter voltages of IGBTs are compared with several preset thresholds to obtain the necessary criterion; and the pulsewidths of the current sources are controlled for gate-loop compensation. Both ADCs and DACs are avoided.

3) The control law is easy to implement in FPGA, and is robust to voltage variation in the power-loop. The voltage unbalancing can be alleviated immediately at the present switching cycle, and further eliminated cycle-by-cycle.

The rest of this paper is organized as follows. In Section II, the voltage unbalancing of IGBTs induced by inconsistent gate-loops is first analyzed, and then the key control criterion is introduced. In Section III, the proposed plug-in gate-loop compensator is designed. In Section IV, the experimental results of two IGBTs in series are given. In Section V, the conclusion is given.

II. ANALYSIS OF IGBTs IN SERIES

The simplified diagram of the SSFCL is shown in Fig. 2, where two IGBTs S_x ($x = a, b$) are series-connected, and two resistors $R_{s(x)}$ ($x = a, b$) are in parallel with the IGBTs to balance the static voltages; The DC voltage of the distribution network is denoted as V_{dc} , and the line stray inductance

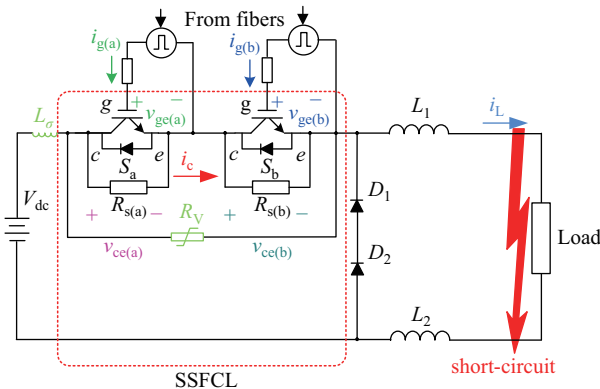


Fig. 2. The simplified diagram of a SSFCL.

is denoted as L_σ . Here, it is assumed that the SSFCL is located close to V_{dc} , thus L_σ is a small value and the stray energy can be dissipated on a power varistor R_v . L_1 and L_2 are the inductances on the transmission lines. If necessary, the extra inductor could be added to limit the slope of the current [25], and the impedance of the transmission line can be ignored compared to that of the inductor. Consequently, the transmission lines are simplified as pure inductive models. D_1 and D_2 are the freewheeling diodes which are used to provide the current paths when the IGBTs are turned off.

As shown in Fig. 3(a), once the short-circuit fault occurs in the load side and the line current i_L reaches the upper threshold current I_{max} , the IGBTs are turned off immediately to prevent the rapid rising of i_L , and then i_L will flow through D_1 and D_2 . When i_L is lower than the lower threshold current I_{min} , the IGBTs are turned on again. Such operations will be repeated for a user-defined period T_{lim} . If the short-circuit is clear within T_{lim} , the IGBTs are constantly turned on again and the distribution network recovers to the normal operation; and if the short-circuit is not clear within T_{lim} , the IGBTs will be constantly turned off to ensure the safety of the network.

During the switching processes, it is important to balance the collector-emitter voltage $v_{ce(a)}$ and $v_{ce(b)}$ of S_a and S_b , respectively. Therefore the mechanism of voltage unbalancing of IGBTs in series is first analyzed. Supposing S_x ($x = a, b$) is driven by the commercial IGBT gate driver without the voltage balancing function, the turning-on process and turning-off process are shown in Fig. 3(b) and (c) respectively, and they are described as follows.

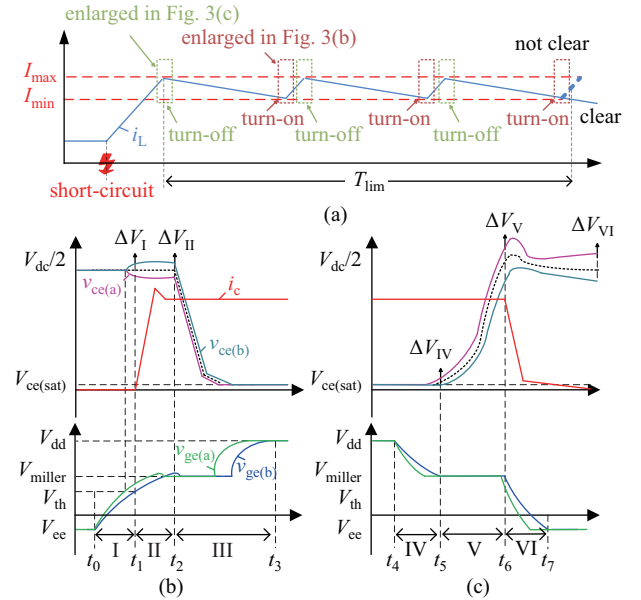


Fig. 3. Working process of SSFCL. (a) Waveform of current limitation. (b) Turning-on process of two series-connected IGBTs. (c) Turning-off process of two series-connected IGBTs.

A. Turning-on Process

Stage I [$t_0 \sim t_1$]: assuming both IGBTs receive the turning-on signal at t_0 , then the gate-emitter voltage $v_{ge(x)}$ ($x = a, b$) of S_x begins to rise from the negative voltage V_{ee} to positive voltage V_{dd} . The gate-loop can be described as a RC circuit

charged by V_{dd} , and $v_{ge(x)}$ can be expressed as:

$$v_{ge(x)}(t - t_0) = V_{dd} + (V_{ee} - V_{dd})e^{-(t-t_0)/\tau_{on(x)}} \quad (1)$$

where $\tau_{on(x)} = R_{on(x)}C_{on(x)}$ ($x = a, b$) is the turning-on time-constant of the gate-loop; $R_{on(x)}$ and $C_{on(x)}$ are the turning-on resistance and capacitance of the gate-loop, respectively.

A slight difference always exists between $\tau_{on(a)}$ and $\tau_{on(b)}$ because 1) tolerance variations of $R_{on(a)}$ and $R_{on(b)}$; 2) $C_{on(x)}$ is dependent on many factors, such as the individual differences of IGBTs and parasitic capacitances from gates to ground [19], and thus $C_{on(a)}$ and $C_{on(b)}$ are not identical as well; 3) device aging can also lead to variations of gate-loop parameters. Therefore, the numerical relationship between $\tau_{on(a)}$ and $\tau_{on(b)}$ is indeterminate. Here the case of $\tau_{on(a)} < \tau_{on(b)}$ (the rising of $v_{ge(a)}$ is faster than that of $v_{ge(b)}$) is taken as an example. Once $v_{ge(a)}$ rises to the threshold voltage V_{th} , S_a enters its active region from the cutoff region while S_b has not yet, which means the on-resistance $r_{s(a)}$ of S_a is decreasing while $r_{s(b)}$ of S_b remains unchanged. Since their sum voltage V_{dc} is constant, $v_{ce(a)}$ is decreasing while $v_{ce(b)}$ is increasing accordingly, so that the unbalancing voltage ΔV_I is introduced.

Stage II [$t_1 \sim t_2$]: at t_1 , $v_{ge(b)}$ also rises to V_{th} so S_b enters its active region. The load current i_L begins to transfer from D_1 and D_2 to S_a and S_b . So i_c , the current flowing through S_a and S_b begins to rise. In this stage, $v_{ce(x)}$ is depending on $r_{s(x)}$, which is given by [20]:

$$r_{s(x)} = v_{ce(x)} / [g_{m(x)}(V_{dd} - i_{g(x)}R_{on(x)} - V_{th})] \quad (2)$$

where $i_{g(x)}$ ($x = a, b$) is the gate current of S_x , $g_{m(x)}$ ($x = a, b$) is the transconductance of S_x .

When the initial voltage deviation ΔV_I is small, the differences between $g_{m(a)}$ and $g_{m(b)}$, $i_{g(a)}$ and $i_{g(b)}$, are small as well, and thus, $r_{s(a)}$ and $r_{s(b)}$ would be similar according to (2). Therefore, the voltage deviation in this stage ΔV_{II} is determined by ΔV_I .

Stage III [$t_2 \sim t_3$]: S_a and S_b enter the Miller plateau in this stage (i.e., $v_{ge(a)} = V_{miller}$ and $v_{ge(b)} = V_{miller}$), so $v_{ce(a)}$ and $v_{ce(b)}$ are decreasing rapidly. The slope of $v_{ce(x)}$ can be expressed as:

$$dv_{ce(x)}/dt = (V_{miller} - V_{dd})/R_{on(x)}C_{gc(x)} \quad (3)$$

where $C_{gc(x)}$ ($x = a, b$) is the gate-collector capacitance of S_x , which depends on $v_{ce(x)}$.

Since $C_{gc(x)}$ is a function of $v_{ce(x)}$ in this stage, $dv_{ce(a)}/dt$ and $dv_{ce(b)}/dt$ would be similar if the voltage deviation of this stage ΔV_{II} was small enough. In brief, if the voltage deviation ΔV_I at the end of stage I can be as small as possible, then the voltage deviations in the following stage II and III can be significantly alleviated, regardless of the difference of $\tau_{(a)}$ and $\tau_{(b)}$.

Therefore, the key criterion of the voltage balancing control for IGBTs is making $\Delta V_I = 0$, in other words, making $v_{ge(a)}$ and $v_{ge(b)}$ rise to V_{th} synchronously.

B. Turning-off Process

Stage IV [$t_4 \sim t_5$]: assuming both IGBTs receive the turning-off signal at t_4 , then $v_{ge(x)}$ begins to fall from V_{dd} to

V_{ee} . The gate-loop can be described as a RC circuit as well, and $v_{ge(x)}$ can be expressed as:

$$v_{ge(x)}(t - t_4) = V_{ee} + (V_{dd} - V_{ee})e^{-(t-t_4)/\tau_{off(x)}} \quad (4)$$

where $\tau_{off(x)} = R_{off(x)}C_{off(x)}$ ($x = a, b$) is the turning-off time-constant of the gate-loop, $R_{off(x)}$ and $C_{off(x)}$ are the turning-off resistance and capacitance of the gate-loop, respectively.

Referring to $\tau_{on(a)}$ and $\tau_{on(b)}$, here $\tau_{off(a)} < \tau_{off(b)}$ is assumed as well, that is, the falling of $v_{ge(a)}$ is faster than that of $v_{ge(b)}$. Once $v_{ge(a)}$ falls to V_{miller} , S_a enters its active region from the saturation region while S_b has not yet, thus $r_{s(a)}$ is increasing while $r_{s(b)}$ remains unchanged. Since the branch of IGBTs in series is conductive, $v_{ce(a)}$ is increasing while $v_{ce(b)}$ remains unchanged. Therefore, the unbalancing voltage ΔV_{IV} is introduced.

Stage V [$t_5 \sim t_6$]: at t_5 , $v_{ge(b)}$ also falls to V_{miller} , thus S_b enters its active regions and $r_{s(b)}$ is increasing. Both $v_{ce(a)}$ and $v_{ce(b)}$ are increasing rapidly, and the slope can be expressed as:

$$dv_{ce(x)}/dt = (V_{miller} - V_{ee})/R_{off(x)}C_{gc(x)} \quad (5)$$

Since $C_{gc(x)}$ is a function of $v_{ce(x)}$ in this stage, the voltage deviation of this stage ΔV_V is further increased by the initial deviation ΔV_{IV} .

Stage VI [$t_6 \sim t_7$]: at t_6 , D_1 and D_2 begin to be conductive, thus i_c is decreasing as $v_{ge(x)}$ is decreasing. When $v_{ge(x)}$ falls to V_{th} , S_x enters the tail current stage, and the two IGBTs in series can be equivalent to the circuit shown in Fig. 4, where $C_{ce(x)}$ ($x = a, b$) is the collector-emitter capacitance of S_x and $i_{tail(x)}$ ($x = a, b$) is the tail current of S_x .

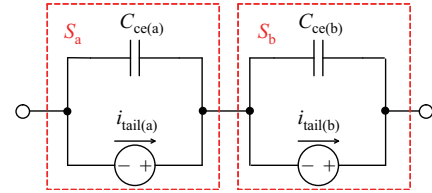


Fig. 4. Equivalent circuit of two series-connected IGBTs in the tail current stage.

Since S_a and S_b are connected in series, the current flowing through S_a is the same as S_b . Therefore, the relationship is approximately expressed as:

$$\begin{cases} i_{tail(x)} = I_{T(x)} \exp(-t/\tau_e) \\ i_c = i_{tail(x)} + C_{ce(x)} dv_{ce(x)}/dt \end{cases} \quad (6)$$

where $I_{T(x)}$ ($x = a, b$) is the initial value of $i_{tail(x)}$ in this stage, and τ_e is the equivalent lifetime of carrier.

According to (6), since the moment of $v_{ge(a)}$ falling to V_{th} is earlier than $v_{ge(b)}$, the decay of $i_{tail(a)}$ is faster than that of $i_{tail(b)}$, and $dv_{ce(a)}/dt$ is greater than $dv_{ce(b)}/dt$. In addition, the voltage deviation ΔV_V exists at the beginning of this stage, therefore, the voltage unbalancing of this stage ΔV_{VI} is further increased.

Consequently, a similar conclusion can also be obtained for the turning-off process, that is, the voltage deviation ΔV_{IV} at the end of stage IV dominates the voltage unbalancing of the

whole turning-off process. Therefore, if $v_{ge(a)}$ and $v_{ge(b)}$ can fall to V_{miller} at the same time, the voltage unbalancing can be greatly reduced as well.

III. THE PROPOSED PLUG-IN GATE-LOOP COMPENSATOR

Based on the above analysis, a FPGA-based parallel plug-in gate-loop compensator with discrete gate voltage feedback and pulsewidth current compensation is proposed, as shown in Fig. 5. $v_{ge(x)} (x = a, b)$ is sent to be compared with several preset thresholds V_α , V_β and V_γ , then the digital outputs (logic “0” or “1”) as control criterion are obtained by FPGA. With the aid of the preset control law, FPGA controls the current sources $I_{p(x)}$ and $I_{n(x)} (x = a, b)$ with “on” or “off” signals to compensate the gate-loop of $S_{(x)} (x = a, b)$. For each IGBT, only four wires (two digital wires for switching signal input and two analog wires integrating $v_{ge(x)}$ sensing and gate current compensation) are required between the proposed gate-loop compensator and the commercial gate driver. Taking the turning-on process as an example, after accurate compensa-

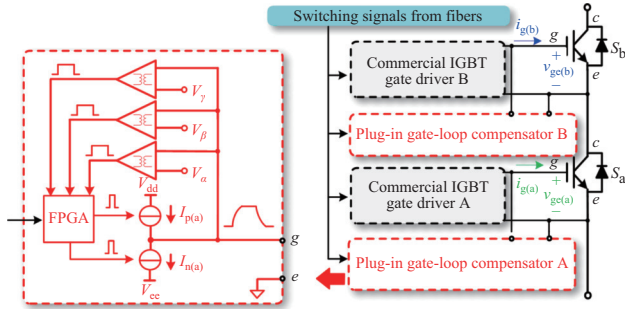


Fig. 5. Function diagram of the proposed gate-loop compensator.

tions of the plug-in gate-loop compensators, $v_{ge(a)}$ and $v_{ge(b)}$ will reach V_{th} synchronously, and the compensation process of S_a is explained in detail, as shown in Fig. 6.

A. Single-cycle Compensation

S1, feedback detection $[t_0 \sim t_{2(a)}]$: at t_0 , $v_{ge(a)}$ begins to rise as the original trend described in (1), and the moment t_0 is recorded by FPGA. When $v_{ge(a)}$ reaches the threshold V_α at $t_{1(a)}$, the output of the isolation comparator is flip-flopped, the moment $t_{1(a)}$ is recorded by FPGA as well. And $\tau_{on(a)}$ is obtained as:

$$\tau_{on(a)} = (t_{1(a)} - t_0) / \ln[(V_{ee} - V_{dd}) / (V_\alpha - V_{dd})] \quad (7)$$

After $t_{1(a)}$, a fix duration T_c is preserved for control action calculation (the calculation will be explained later), and then this stage ends at $t_{2(a)}$.

S2, current compensation $[t_{2(a)} \sim t_{3(a)}]$: according to the calculation result obtained in T_c , FPGA generates a pulsewidth signal with turning on time $T_{p(a)} = t_{3(a)} - t_{2(a)}$ to control $I_{p(a)}$. During this stage, the gate-loop can be equivalent to a RC circuit charged by the voltage source V_{dd} plus $I_{p(a)}$. $v_{ge(a)}$ is given as:

$$v_{ge(a)}(t) = (V_{dd} + R_{on(a)}I_{p(a)}) + [v_{ge(a)}(t_{2(a)}) - V_{dd} - R_{on(a)}I_{p(a)}]e^{-(t-t_{2(a)})/\tau_{on(a)}} \quad (8)$$

S3, non-compensation $[t_{3(a)} \sim t_4]$: since $I_{p(a)}$ compensation is turned off at $t_{3(a)}$, the gate-loop goes back to a RC circuit charged by V_{dd} , and $v_{ge(a)}$ which can be given as:

$$v_{ge(a)}(t) = V_{dd} + [v_{ge(a)}(t_{3(a)}) - V_{dd}]e^{-(t-t_{3(a)})/\tau_{on(a)}} \quad (9)$$

In order to make $v_{ge(a)}(t)$ reach V_{th} at t_4 , $T_{p(a)}$ needs to be calculated during the preserved period T_c . Using the condition

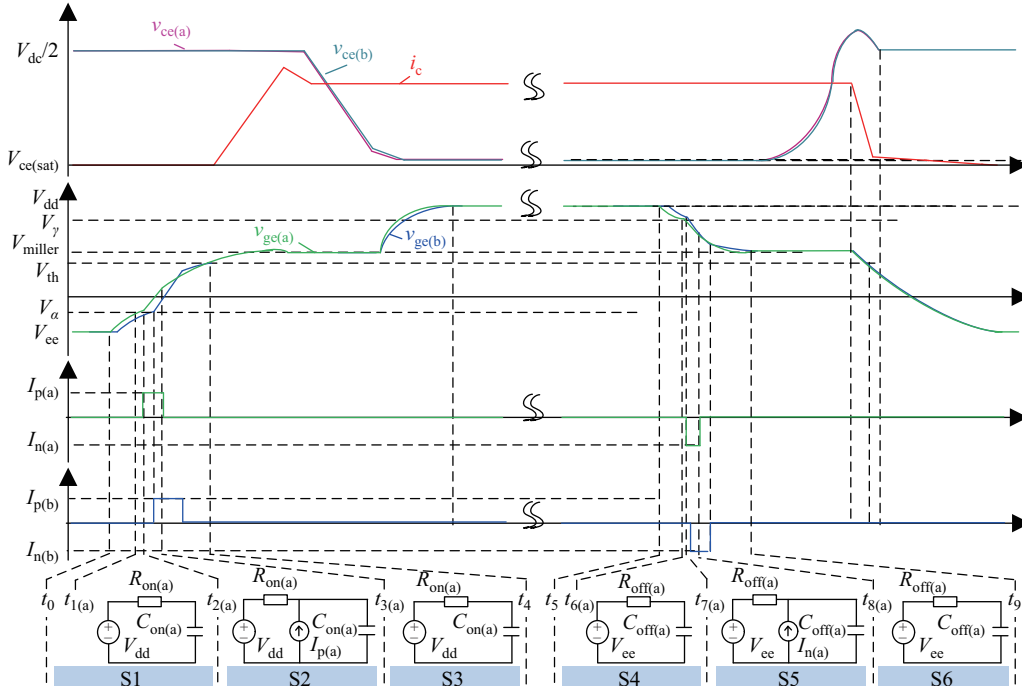


Fig. 6. Switching waveforms of two series-connected IGBTs with the proposed gate-loop compensators.

$V_{th} = v_{ge(a)}(t_4)$ and substituting (8) into (9) gives:

$$T_{p(a)} = \tau_{on(a)} \ln \frac{(V_{th} - V_{dd})/e^{(-t_4 + t_{2(a)})/\tau_{on(a)}} - [v_{ge(a)}(t_{2(a)}) - V_{dd} - R_{on(a)}I_{p(a)}]}{R_{on(a)}I_{p(a)}} \quad (10)$$

In (10), V_{dd} , V_{th} , $I_{p(a)}$ and t_4 are preset; $R_{on(a)}$ can be obtained from the manual of the commercial driver (the tolerance variation is so small that its effect on the calculation result can be ignored, and $R_{on(a)}$ is considered as a constant, which is further clarified in the following Section IV); since $t_{1(a)}$ is recorded by FPGA, $t_{2(a)} = t_{1(a)} + T_c$ can be calculated; $\tau_{on(a)}$ can be solved by (7) and $v_{ge(a)}(t_{2(a)})$ can be solved by (1). In brief, $T_{p(a)}$ can be calculated since all the parameters are known.

In a similar manner, the IGBT S_b is also controlled by its plug-in gate-loop compensator, and the computed pulse width $T_{p(b)}$ for current compensation has a similar form as (10).

B. Cycle-by-cycle Compensation

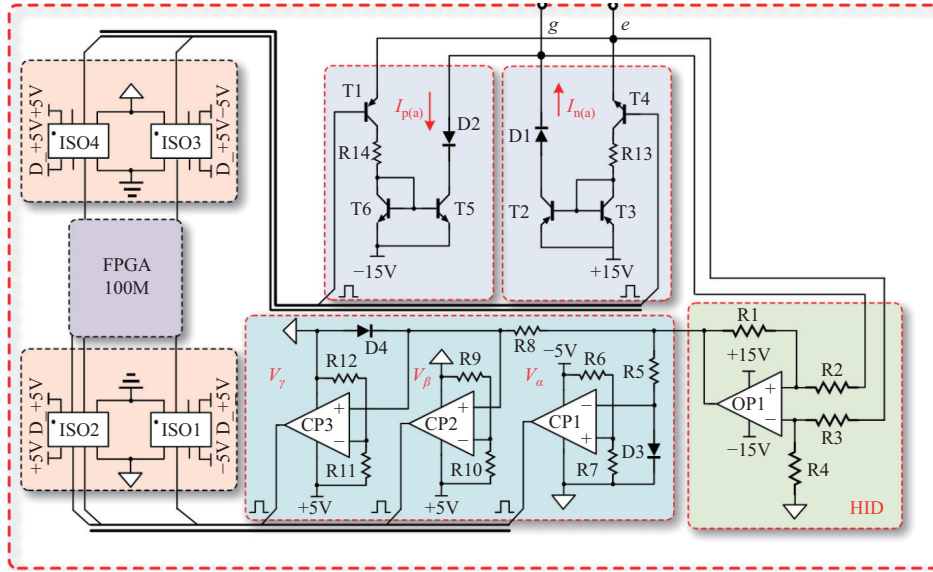
However, many unideal factors, such as inaccurate parameters, make $T_{p(a)}$ and $T_{p(b)}$ deviate from their ideal values,

and thus, $v_{ge(a)}$ and $v_{ge(b)}$ cannot reach V_{th} at t_4 perfectly in a single-cycle regulation. To compensate for these factors, a cycle-by-cycle regulation is added, by fully utilizing the PWM operation of SSFCL during the period T_{lim} . $v_{ge(x)}$ is compared with $V_\beta = V_{th}$, and when $v_{ge(x)}$ reaches V_β , the flip-flop moment $t_{4(x)}(x = a, b)$ is recorded by FPGA, and a cycle-by-cycle control is designed:

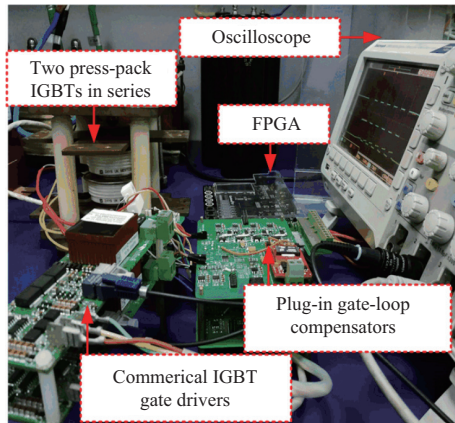
$$T_{p(x)}[n+1] \leftarrow T_{p(x)}[n+1] + k \cdot \text{sum}[n] \quad (11)$$

where $\text{sum}[n]$ is the integral of $\Delta t[n]$ over n cycles, in which $\Delta t[n]$ is the error of $t_{4(a)}$ and $t_{4(b)}$ in the n -th switching cycle; k is the integral coefficient, which is selected based on the experimental results under low voltage conditions, and then is fine-tuned when the voltage is increased gradually; $T_{p(a)}[n+1]$ is the pulse width of the compensation current that will be calculated in the next switching cycle.

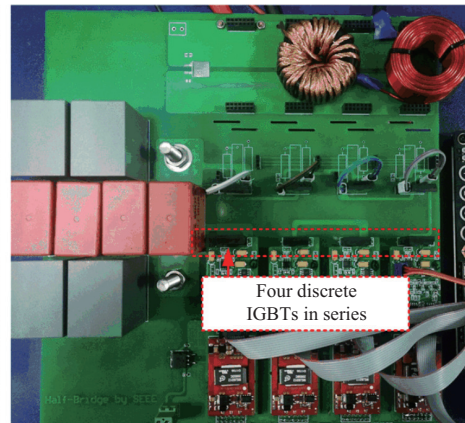
In this way, $\Delta t[n]$ introduced by the unideal factors will be gradually compensated in the next switching cycle, and finally $v_{ge(a)}$ and $v_{ge(b)}$ can reach V_{th} synchronously.



(a)



(b)



(c)

Fig. 7. Prototype design. (a) Details of proposed gate-loop compensator. (b) Test bench of two series-connected press-pack IGBTs. (c) Test bench of four series-connected discrete IGBTs.

IV. EXPERIMENTAL RESULTS

A. Experimental Scale-down Platform

The detail of the proposed plug-in gate-loop compensator is shown in Fig. 7(a). A high impedance differential circuit (HID) is utilized to sense $v_{ge(x)}$, and then $v_{ge(x)}$ is sent to several comparators (CP1 ~ CP3) for comparisons. The outputs of the comparators are sent to FPGA via digital isolators (ISO1, SIO2) for compensation. The compensation signals generated by FPGA are pulsewidth signals, which are used to drive the current sources $I_{p(x)}$ and $I_{n(x)}$ via digital isolators (ISO3, SO4). FPGA with 100 MHz is chosen as the control core. As shown in Table I, the parameters of the key devices are given.

TABLE I
KEY DEVICES OF COMPENSATORS AND THEIR PARAMETERS

Name	Parameter
FPGA	EP4CE10F17C8 N
OP1	LM6172
T1 ~ T3	MMBT2369A
T4 ~ T6	MMBT5771
D1 ~ D4	1 N4002
C1 ~ C3	ADCM600
ISO1 ~ ISO4	SI8410

The applied IGBT in SSFCL needs to be selected according to the actual working conditions. The voltage rating V_{ce} of a single IGBT is defined as:

$$V_{ce} = K_V \times (L_\sigma \times di_c/dt + V_{dc})/n = K_V \times (V_\sigma + V_{dc})/n \quad (12)$$

where the series-connected IGBTs withstand the superimposed voltage of DC bus voltage V_{dc} and voltage overshoot V_σ during the turning-off process; n is the number of applied IGBTs; K_V is a margin coefficient which is greater than one by taking the worse working condition into consideration.

As for the current rating I_c , it needs to be chosen according to the load current I_L under the normal working conditions of the system, that is, the SSFCL is in a constant on state. In addition, since there are several large current pulses flowing through IGBTs in SSFCL when the short-circuit occurs, another parameter named pulsed collector current I_{cpuls} should be selected according to the upper threshold current I_{max} . I_c and I_{cpuls} are defined as:

$$\begin{cases} I_c = K_I \times I_L \\ I_{cpuls} = K_I \times I_{max} \end{cases} \quad (13)$$

where K_I is greater than one as well considering the current margin.

In order to verify our design, two prototypes are designed. 1) To illustrate the advantages of the proposed gate-loop compensator, two press-pack IGBTs from IXYS are used. Due to the wireless and solderless bond structures, press-pack IGBTs inherit the highly consistent power-loops, and this makes us focus on the voltage unbalancing induced by inconsistent gate-loops. And the matched commercial IGBT gate driver boards are used. They provide the high driving power and full protection function, ensuring the safety of the IGBTs, and the proposed gate-loop compensator can be easily

cooperated with it. 2) To test the robustness of the proposed method, four discrete IGBTs from Infineon are applied, and the commercial gate driver chips are matched with the IGBTs. The detail is given in Table II. It is noted that, the IGBT's rated parameters are with large margins in our design for safety purposes. The test platforms are established respectively as shown in Fig. 7(b) and Fig. 7(c).

TABLE II
IGBTS AND THEIR GATE DRIVERS

Name	Parameter
Press-pack IGBT	T0360NB25A (2500V/360A)
Gate driver board	C0044BG400SBA
Discrete IGBT	IHW50N65R5 (650V/50A)
Gate driver chip	SI8271

Since the parameter identification is implemented by FPGA in the compensator, and current source compensations are controlled by FPGA as well, sufficient accuracy and fast response need to be guaranteed. If not, the voltage balancing effect of the compensators would be unsatisfied. Consequently, to realize the proposed control, two optimizations are designed:

1) In our case, each clock cycle of FPGA is 10 ns. It means the resolution of captured timings, such as $t_{1(x)}$ and $t_{4(x)}$, is 10 ns, which is not enough for compensation (the available period for control of a press-pack IGBT is about 700 ns). Therefore, four 200 MHz PLL clocks, whose phases are sequentially lagged by 90 degrees, are structured to increase the resolution of the capture timings. The resolution is thus improved to 1.25 ns.

2) Equations (7)–(10) are too complicated to be calculated in such a short period T_c . Fortunately, regarding t_0 as zero, the required $T_{p(a)}$ in (10) is only dependent on $t_{1(a)}$ in real time, while the rest of the parameters are known. As shown in Fig. 8 where press-pack IGBTs are applied, since the variation of $R_{on(a)}$ has very limited impact on $T_{p(a)}$ (it is seen that when $R_{on(a)}$ varies from 8.7 to 9.5 Ω , the curves are almost identical), all possible pairs of $[t_{1(a)}, T_{p(a)}]$ can be solved offline, and then stored in a look-up table in FPGA. Once $t_{1(a)}$ is captured, the corresponding $T_{p(a)}$ is indexed within only 2 clock cycles, and thus, it can be implemented during the preserved period T_c .

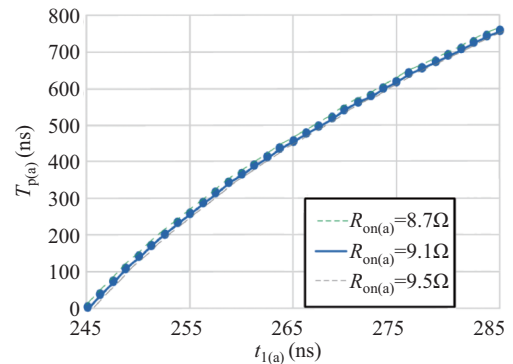


Fig. 8. Correspondence between $T_{p(a)}$ and $t_{1(a)}$.

B. Experimental Results of Two Press-Pack IGBTs in Series

The detailed experimental results of two series-connected press-pack IGBTs are shown first. Figs. 9 (a) and (b) give

the comparison between gate driver sides without and with compensation during the turning-on process. In Fig. 9(a), the proposed gate-loop compensator is disabled, $v_{ge(a)}$ rises at t_0 and reaches V_{th} after 680 ns. In Fig. 9(b), when $v_{ge(a)}$ reaches V_{α} at $t_{1(a)}$, the digital logic to FPGA is flip-flopped from “1” to “0” and then the required $T_{p(a)} = 200$ ns is indexed from the look-up table during T_c , then a current $i_{p(a)}$ with 200 ns pulse width is compensated to the gate-loop. After compensation, the time of $v_{ge(a)}$ rising to V_{th} is shortened to 640 ns. In the same manner, the time of $v_{ge(a)}$ falling to V_{miller} during the turning-off process is shortened from 640 ns to 560 ns, as shown in Figs. 10(a) and (b), respectively. These experiments show that the proposed gate-loop compensator can fine-tune the state of the gate-emitter voltage, and thus, can control the voltage balancing of IGBTs. Taking the typical compensation duration of 200 ns and the compensation current of 260 mA during both the turn-on and turn-off process as examples, the power

consumption of the compensator is 3.12 μ J per switching cycle, while the power consumption of the commercial gate driver is 90 μ J. Therefore, the power consumption of the compensator only accounts for 3.47% of the commercial gate driver.

In the case where $V_{dc} = 1000$ V (the maximal voltage in our test bench, which is limited by the condition of the lab), when the short-circuit occurs, S_a and S_b are forced to be turned off. As shown in Fig. 11(a), when no gate-loop compensation is applied, the voltage unbalancing of the power sides occurs during the turning-off process; in contrast, as shown in Fig. 11(b), when the proposed compensation (only the single-cycle compensation part) is added, $v_{ce(a)}$ and $v_{ce(b)}$ are substantially balanced. Similarly, when S_a and S_b are turned on without gate-loop compensation, as shown in Fig. 12(a), $v_{ce(a)}$ and $v_{ce(b)}$ are unbalanced; while in Fig. 12(b), $v_{ce(a)}$ and

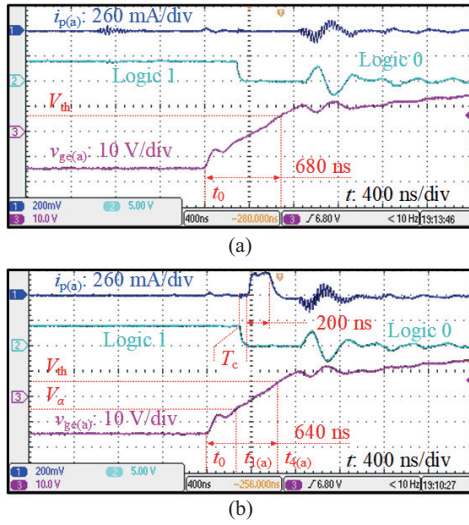


Fig. 9. Experimental waveforms of gate driver sides during turning-on process. (a) Without compensator. (b) With compensator.

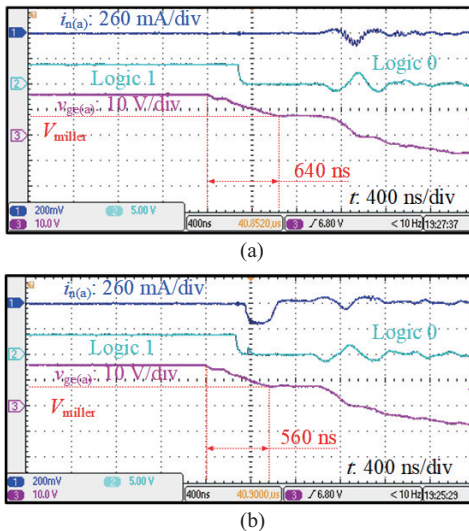


Fig. 10. Experimental waveforms of gate driver sides during turning-off process. (a) Without compensator. (b) With compensator.

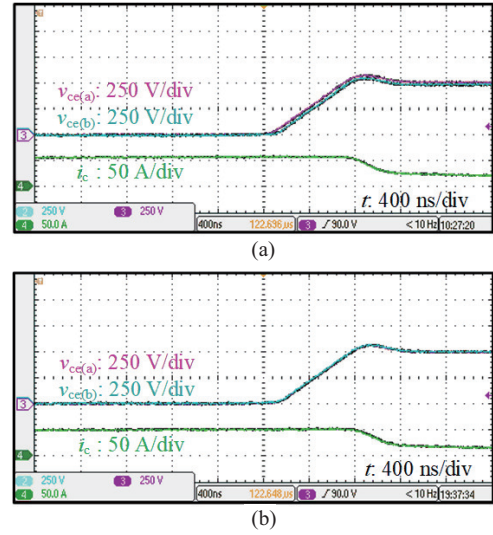


Fig. 11. Experimental waveforms of power sides during turning-off process. (a) Without compensator. (b) With single-cycle compensation.

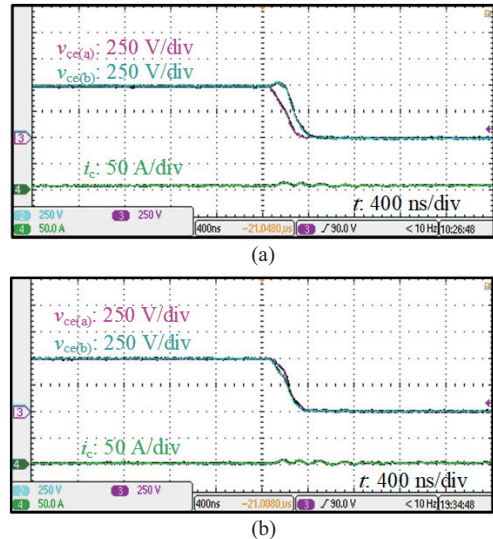


Fig. 12. Experimental waveforms of power sides during turning-on process. (a) Without compensator. (b) With single-cycle compensation.

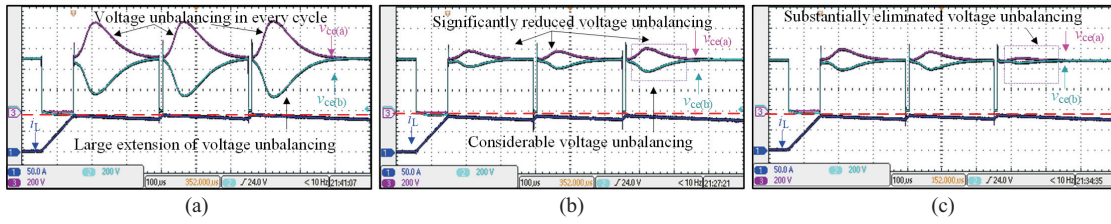


Fig. 13. Experimental results of two series-connected press-pack IGBTs when $V_{dc} = 1000$ V ($v_{ce(a)}$, $v_{ce(b)}$: 200V/div, i_L : 50 A/div, t : 100 μ s/div). (a) Without compensation. (b) With single-cycle compensation. (c) With single-cycle and cycle-by-cycle compensations.

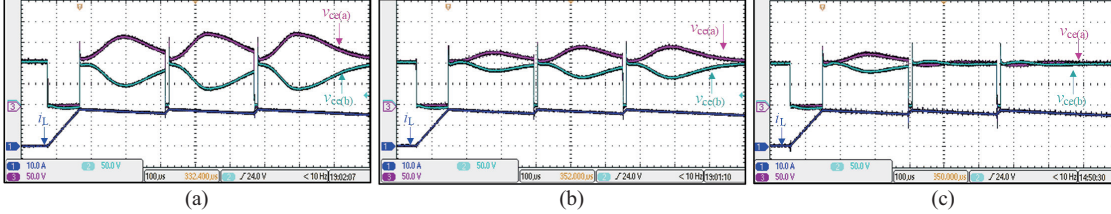


Fig. 14. Experimental results of two series-connected press-pack IGBTs when $V_{dc} = 200$ V ($v_{ce(a)}$, $v_{ce(b)}$: 50 V/div, i_L : 10A/div, t : 100 μ s/div). (a) Without compensation. (b) With single-cycle compensation. (c) With single-cycle and cycle-by-cycle compensations.

$v_{ce(b)}$ are well balanced with the proposed compensation (only the single-cycle compensation part). These experiments show that during the switching process, $v_{ce(a)}$ and $v_{ce(b)}$ can be well balanced with the single-cycle compensation.

However, a considerable voltage unbalancing still exists since the single-cycle compensation is not completely accurate due to the non-ideal factors. Such a voltage unbalancing will be eliminated by the proposed cycle-by-cycle compensation, and this can be verified by observing the working processes of SSFCL without and with the proposed gate-loop compensator which are compared in the following section.

In Fig. 13(a), the two IGBTs are only driven by the commercial drivers under $V_{dc} = 1000$ V without gate-loop compensation. Although the current can be limited at 90 A, distinct voltage unbalancing can be observed in every switching cycle. Especially, such a voltage unbalancing has a large extension when the IGBTs are constantly off. To facilitate the analyzation, the degree of voltage unbalancing is calculated as 70% (the maximal $|v_{ce(a)} - v_{ce(b)}| / |v_{ce(a)} + v_{ce(b)}|$ during the third off period). In Fig. 13(b), only the proposed single-cycle compensation is enabled. It is seen that the voltage unbalancing in every switching cycle is significantly reduced. However, a small voltage unbalancing still remains, resulting in a considerable 20% voltage unbalancing extension when the IGBTs are constantly off. In Fig. 13(c), the proposed cycle-by-cycle compensation is further added. It is seen that the voltage unbalancing is substantially eliminated after several switching cycles, even when the IGBTs are constantly off.

To show the robustness of the proposed gate-loop compensation, Fig. 14 shows the experimental waveforms when $V_{dc} = 200$ V. Without the proposed plug-in gate-loop compensator, voltage unbalancing is still significant even if V_{dc} is low; while with the proposed compensator, single-cycle compensation can reduce voltage unbalancing from 65% to 37.5%; the addition of cycle-by-cycle compensation can further reduce the voltage unbalancing to be within 5%.

C. Experimental Results of Four Discrete IGBTs in Series

To further verify the proposed voltage balancing control with compensation, the case of four series-connected discrete IGBTs is considered. In the $V_{dc} = 600$ V case, the voltage sharing of IGBTs without and with compensations are given in Fig. 15(a) and (b), respectively. It is concluded that the voltages of four IGBTs are well balanced after compensation. The same conclusion is obtained under $V_{dc} = 200$ V, as shown in Fig. 16, which verifies the robustness of the proposed compensators. However, it should be noted that with the increase of the number of series-connected IGBTs, the parameter accuracy requirements are higher, and the control becomes more complicated, which influences the voltage balancing of the proposed gate-loop compensators, and this factor should be considered during design.

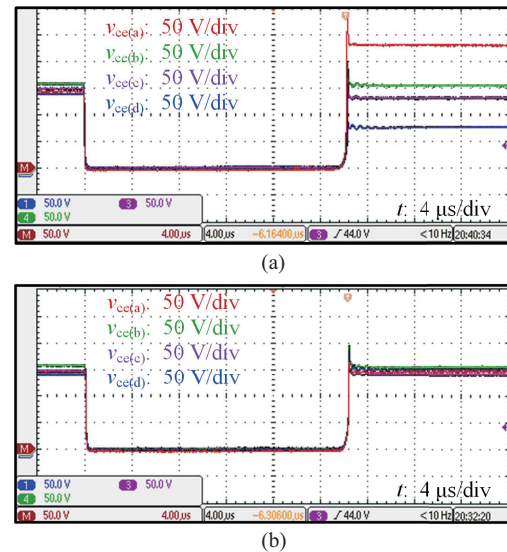


Fig. 15. Experimental results of four series-connected IGBTs under $V_{dc} = 600$ V. (a) Without compensator. (b) With compensator.

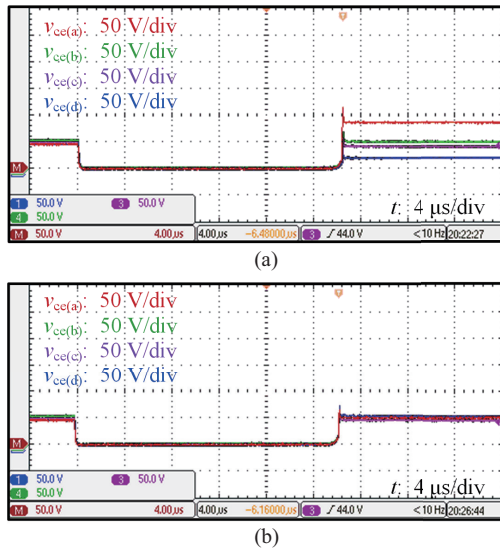


Fig. 16. Experimental results of four series-connected IGBTs under $V_{dc} = 200$ V. (a) Without compensator. (b) With compensator.

D. Discussion

The performance of the proposed compensator can be further improved as follows:

1) In addition to structuring four PLL clocks and storing look-up tables in FPGA, a FPGA with higher frequency can be chosen to improve the accuracy and response speed. In addition, the comparators and their layouts should be optimized to reduce signal delay.

2) The compensator needs a period of time for parameter identification and another period of time for current source compensation. Therefore, a certain turn-on delay time and turn-off delay time are required. Consequently, the gate resistance should be selected based on the input capacitance of the adopted IGBT. Such a way may cause higher switching loss in every switching cycle. However, since only several switching pulses are applied to SSFCL when short-circuit fault occurs, it is well suited for SSFCL.

V. CONCLUSION

In this paper, the voltage unbalancing of series-connected IGBTs in a SSFCL is discussed. First the switching processes of the series-connected IGBTs are analyzed, and the key criterion for gate-loop compensation is given. It is concluded that if the gate-emitter voltages of IGBTs can reach the threshold/miller voltage synchronously, then the voltage unbalancing induced by inconsistent gate-loops would be greatly reduced.

Therefore, a plug-in gate-loop compensator with discrete feedback and pulse width current compensation is proposed. The proposed compensator compares the gate-emitter voltage with several thresholds, and then controls the pulse width of the compensation current without ADCs and DACs.

A design example shows that the circuit is simple since only 3 comparators and 4 isolators are used. By storing a look-up table in FPGA, the pulsewidth of the compensation current can be calculated and indexed within 2 clock cycles; by structuring the PLL clocks, the resolution of the captured

timings is improved from 10 ns to 1.25 ns; and the power of the compensation current only accounts for 3.47% of the driving power.

The experimental results of two series-connected press-pack IGBTs show the single-cycle compensation can reduce voltage unbalancing from 70% to 20% if the DC voltage is 1000 V, and the addition of cycle-by-cycle compensation can further reduce the voltage unbalancing to 5%. And voltage unbalancing can always be limited within 5% when DC voltage varies in a wide range. In addition, the experimental results of four discrete IGBTs connected in series also show good voltage balancing with the compensator despite the control becomes much more complicated, which further verifies the effectiveness of the proposed compensator.

REFERENCES

- [1] N. Chen, L. Qi, Y. Tang, C. Y. Zhao, X. Cui, and C. Gao, "Two-port equivalent circuit model for UHVDC converter valves," *CSEE Journal of Power and Energy Systems*, vol. 5, no. 1, pp. 100–110, Mar. 2019.
- [2] A. Abramovitz and K. Ma Smedley, "Survey of solid-state fault current limiters," *IEEE Transactions on Power Electronics*, vol. 27, no. 6, pp. 2770–2782, Jun. 2012.
- [3] L. Qi, J. Pan, X. Huang, and X. Feng, "Solid-state fault current limiting for DC distribution protection," in *Proceedings of 2017 IEEE Electric Ship Technologies Symposium*, Arlington, VA, 2017, pp. 187–191.
- [4] H. Pang, J. L. Wen, Z. Y. He, and G. F. Tang, "Unbalancing voltage of high power series connected IGBT valve," *Proceedings of the CSEE*, vol. 31, no. 21, pp. 1–8, Jul. 2011.
- [5] T. C. Lim, B. W. Williams, and S. J. Finney, "Active snubber energy recovery circuit for series-connected IGBTs," *IEEE Transactions on Power Electronics*, vol. 26, no. 7, pp. 1879–1889, Jul. 2011.
- [6] R. Withanage and N. Shammass, "Series connection of Insulated Gate Bipolar Transistors (IGBTs)," *IEEE Transactions on Power Electronics*, vol. 27, no. 4, pp. 2204–2212, Apr. 2012.
- [7] J. W. Baek, D. W. Yoo, and H. G. Kim, "High-voltage switch using series-connected IGBTs with simple auxiliary circuit," *IEEE Transactions on Industry Applications*, vol. 37, no. 6, pp. 1832–1839, Nov./Dec. 2001.
- [8] C. Abbate, G. Busatto, and F. Iannuzzo, "High-voltage, high-performance switch using series-connected IGBTs," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2450–2459, Sep. 2010.
- [9] A. Bagheri, H. Iman-Eini, and S. Farhangi, "A gate driver circuit for series-connected IGBTs based on quasi-active gate control," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 791–799, Jun. 2018.
- [10] N. Teerakawanich and C. M. Johnson, "Design optimization of quasi-active gate control for series-connected power devices," *IEEE Transactions on Power Electronics*, vol. 29, no. 6, pp. 2705–2714, Jun. 2014.
- [11] D. V. M. M. Krishna and V. Agarwal, "Active gate control of series connected IGBTs using positive current feedback technique," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 5, pp. 261–265, May 2005.
- [12] A. Raciti, G. Belverde, A. Galluzzo, G. Greco, M. Melito, and S. Musumeci, "Control of the switching transients of IGBT series strings by high-performance drive units," *IEEE Transactions on Industrial Electronics*, vol. 48, no. 3, pp. 482–490, Jun. 2001.
- [13] G. Belverde, A. Galluzzo, M. Melito, S. Musumeci, and A. Raciti, "Snubberless voltage sharing of series-connected insulated-gate devices by a novel gate control strategy," *IEEE Transactions on Power Electronics*, vol. 16, no. 1, pp. 132–141, Jan. 2001.
- [14] P. R. Palmer and H. S. Rajamani, "Active voltage control of IGBTs for high power applications," *IEEE Transactions on Power Electronics*, vol. 19, no. 4, pp. 894–901, Jul. 2004.
- [15] R. Wang, L. Liang, Y. Chen, Y. Pan, J. Y. Li, L. B. Han, and G. Q. Tan, "Self-adaptive active gate driver for IGBT switching performance optimization based on status monitoring," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 6362–6372, Jun. 2020.
- [16] T. C. Lim, B. W. Williams, S. J. Finney, and P. R. Palmer, "Series-connected IGBTs using active voltage control technique," *IEEE Transactions on Power Electronics*, vol. 28, no. 8, pp. 4083–4103, Aug. 2013.

- [17] T. Lu, Z. M. Zhao, S. Q. Ji, H. L. Yu, and L. Q. Yuan, "Active clamping circuit with status feedback for series-connected HV-IGBTs," *IEEE Transactions on Industry Applications*, vol. 50, no. 5, pp. 3579–3590, Sep./Oct. 2014.
- [18] S. Q. Ji, T. Lu, Z. M. Zhao, H. L. Yu, and L. Q. Yuan, "Series-connected HV-IGBTs using active voltage balancing control with status feedback circuit," *IEEE Transactions on Power Electronics*, vol. 30, no. 8, pp. 4165–4174, Aug. 2015.
- [19] K. Sasagawa, Y. Abe, and K. Matsuse, "Voltage-balancing method for IGBTs connected in series," *IEEE Transactions on Industry Applications*, vol. 40, no. 4, pp. 1025–1030, Jul./Aug. 2004.
- [20] A. Marzoughi, R. Burgos, and D. Boroyevich, "Active gate-driver with dv/dt controller for dynamic voltage balancing in series-connected SiC MOSFETs," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 4, pp. 2488–2498, Apr. 2019.
- [21] I. Baraia, J. A. Barrena, G. Abad, J. M. C. Segade, and U. Iraola, "An experimentally verified active gate control method for the series connection of IGBT/diodes," *IEEE Transactions on Power Electronics*, vol. 27, no. 2, pp. 1025–1038, Feb. 2012.
- [22] F. Zhang, X. Yang, Y. Ren, Y. Chen, and R. F. Gou, "Voltage balancing circuit for series-connected IGBTs in solid-state breaker," *Proceedings of the CSEE*, vol. 36, no. 3, pp. 656–663, Feb. 2016.
- [23] G. Chen, Y. Wang, and X. Cai, "A novel serial hybrid three-level NPC topology for multi-MW medium voltage wind power converters," *Proceedings of the CSEE*, vol. 33, no. 9, pp. 48–54, Mar. 2013.
- [24] F. Zhang, X. Yang, Y. Ren, L. Feng, W. J. Chen, and Y. Q. Pei, "A hybrid active gate drive for switching loss reduction and voltage balancing of series-connected IGBTs," *IEEE Transactions on Power Electronics*, vol. 32, no. 10, pp. 7469–7481, Oct. 2017.
- [25] Y. Du, J. P. Deng, H. Y. Lin, H. Zheng, K. L. Xiang, and Y. Shen, "Research and experiment of a current-limiting HVDC circuit breaker," *The Journal of Engineering*, vol. 2019, no. 16, pp. 2002–2006, Apr. 2019.



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